In the Specification:

Please replace the following amended paragraphs:

Page 1, paragraph 3, lines 9 to 13 insert the following paragraph:

This application is related to applications filed on the same day by the same inventors under (Attorney Docket 85195-602 ADB), Serial No. 10/796,415, entitled APPARATUS FOR FRACTIONAL RF SIGNAL SYNTHESIS WITH PHASE MODULATION and (Attorney Docket 85195-402 ADB), Serial No. 10/796,417, entitled METHOD AND APPARATUS FOR FRACTIONAL RF SIGNAL SYNTHESIS the disclosures of which are incorporated herein by reference.

Page 3, paragraph 7, lines 8 to 10 insert the following paragraph:

The reference clock frequency divided by the desired output frequency multiplied by 2^n ~~2^n~~ multiplied by (p/100), where p is the percentage duty cycle and n is the number of bits in the accumulator math.

Page 3, paragraph 9, lines 13 to 14 insert the following paragraph:

The reference frequency divided by 2^n ~~2^n~~, where n is equal to the number of bits in the accumulator.

Page 3, paragraph 13, lines 21 to 22 insert the following paragraph:

Preferably the interpolator is a (sin x)/x ~~sin x/x~~ interpolator filter.

The paragraph bridging pages 6 and 7, page 6, paragraph 9, lines 17 to 23 and page 7, paragraph 1, lines 1 to 25, insert the following paragraph.

A prior art, architecture 15 for a QAM modulator 17 is shown in Figure 1. The modulator 17 accepts a digital input 19 which is fed to an encoder 23. The encoder 23 divides the incoming signal into a symbol constellation corresponding to in-phase (I) ($x_r(nT)$) and quadrature (Q) ($jx_i(nT)$) phase components while also performing forward error correction (FEC) required for subsequent decoding in the demodulator. The converter's outputs are fed to the two identical finite impulse response (FIR) square-root raised Nyquist matched filters 25, 27. These Nyquist filters 25, 27 are a pair of identical interpolating low-pass filters which receive the I ($x_r(nT)$) and Q ($jx_i(nT)$) signals from the encoder 23 and generate real and imaginary parts of the complex band-limited baseband signal. The Nyquist filters 25, 27 ameliorate intersymbol interference (ISI) which is a by-product of the amplitude modulation with constrained bandwidth. After filtering, the in-phase ($y_r(nT')$) ~~($(y_r(nT'))$~~ and quadrature ($y_i(nT')$) components are multiplied 29, 31 with the IF centered carrier signals 33, 35. The multiplied signals are then summed 37 producing a band limited IF QAM output signal ($g(nT)$). The digital signal is then converted to an analog signal using a D/A converter 39. The analogue signal is processed 40 ~~41~~ and fed to a linear power amplifier 41 for amplification and transmission at 42. Due to the limited frequency range of the D/A converter 39, the analog signal processing 40 may also contain upconversion to convert the IF frequency from the D/A output 39 to

an RF frequency signal. This method requires a large, very linear power amplifier as the modulation must be produced at low power. This consequently results in very poor power efficiency.

Page 8, paragraph 2, lines 6 to 21 insert the following paragraph:

The device delays an edge of the reference clock by an amount which is controlled by the modulation adder ~~102~~ 102a, 102b and implemented by the programmable delay ~~106~~ 106a, 106b. The reference edge could be either the rising or falling edge of the reference clock. There are separate circuits for the control of the two edges so that the rising and falling edge of the output signal 150 can be independently controlled. This ensures that even if the duty cycle of the input reference is not 50%, the output 150 duty cycle can be controlled as both the rising edge and falling edge delay is triggered from the same edge of the reference clock 103. The desired output duty cycle is typically 50% to maximize the RF power in the fundamental frequency but any desired duty cycle can be achieved. Duty cycle is controlled by setting the initial value ~~111~~ 111a, 111b. The frequency of the RF output is selected by loading the increment value 100. The operation is controlled by two equations. The first equation controls the RF output frequency and it determines the value to be loaded in the increment value register 101. Given that the high speed adder/accumulator ~~102~~ 102a, 102b is comprised of 2^n ~~2^n~~ bits, where n is the number of bits in the accumulator math, the increment value 101 is given by the following equation:

Page 9, paragraph 4, lines 9 to 15 insert the following

paragraph:

The second equation controls the duty cycle of the output. As shown in Figure 2, there are separate blocks to control the rising edge delay (a) and the falling edge delay (b). To accomplish a fixed duty cycle, the increment values ~~101a~~ 101 ~~and 101b~~ must be the same and the initial start up values 111a and 111b in the accumulator must be set to provide for the desired fixed delay between them. The equation for the initializing value 111b assuming the initializing value for 111a to be zero is as follows:

The paragraph bridging pages 9, 10 and 11, page 9 , paragraph 9, lines 21 to 23 and page 10, paragraph 1, lines 1 to 23 and page 11, paragraph 1, lines 1 to 19 insert the following paragraph.

For the example shown in Table 1, for duty cycle p = 50 %, the initializing value 111b is calculated to be 2789. Table 1 illustrates that the adder/accumulator 102a starts at 0 and increments 1482 at every rising edge of the clock. At the same time adder/accumulator 102b starts at 2789 and increments 1482 every rising edge of the clock. Any phase modulation required is added in a second modulation adder 120. When the modulation adder 120 overflows and produces a carry out due to the math addition, an input pulse edge must be ignored or "swallowed". This corresponds to phase wraparound, i.e. the phase shift has reached 360 degrees and must be set to 0 degrees. In the present invention, 2^n ~~2^n~~ is calibrated to equal 360 degrees of the reference clock input 103. This calibration is performed in the LUT ~~105~~ 105a, 105b by a simple mapping of input control bits to desired control lines. The filling of the

LUT ~~105~~ 105a, 105b to perform this requirement would be well understood by those skilled in the art. The LUTs ~~105~~ 105a, 105b can be implemented using a read only memory or with a microprocessor. The adder/accumulator overflows due to an addition indicates a greater than 360 degree delay requirement. This delay is implemented by using the next clock edge rather than delaying from the original clock edge. This allows the programmable delay line ~~106~~ 106a, 106b to act as a delay line with endless delay capability. For example if the accumulator is using 12 bit math then 360 degrees is equal to 2^{12} ~~2^12~~ or 4096 . In the example shown in Table 1, the accumulator overflows to 4446, which means the overflow bits are set to a value of 1 and accumulator value goes to 4446 – 4096 = 350. The circuit implements the requirement for this value of phase delay in two parts. It activates the pulse swallow circuit to ignore one clock edge, and sets the programmable delay to 350 which completes the rest of the delay requirement. This unique feature of the present invention means that any quantity of overflow bits could be handled. If the addition of the increment value 101 to the accumulator value ~~102~~ 102a, 102b causes, for example, two overflow bits, then the pulse swallow circuit ~~104~~ 104a, 104b at the output 112 of the accumulator 102a, 102b would ignore or "swallow" 2 pulses. In this way it is possible to synthesis very low frequencies ~~108~~ from the high speed clock reference 103. The delay required to achieve this is limited to one cycle at the high speed reference clock rate. Furthermore, the accuracy of the timing and jitter is excellent, as the time is always relative to the closest edge of the high speed clock reference 103. The output signal phase noise is not controlled by

the loop bandwidth nor the phase noise characteristics of the voltage controlled oscillators applied in traditional methods. Instead, the phase noise performance is directly linked to the high speed reference. This reduces both the jitter and phase noise of the synthesized RF output ~~108~~. The delayed edge from the programmable delay 106a sets the output RF high ~~108~~ by enabling a set-reset flipflop 107. When the delayed edge from the programmable delay 106b reaches the flipflop, it resets the flip flop 107 and causes the RF output ~~108~~ to go low. This completes the synthesis of the RF output ~~108~~ at the preferred 50% duty cycle rate. Figure 6 illustrates time plots for the example in Table 1. The upper plot is the high speed reference clock plotted over 5500 degrees. The lower plot is the RF output ~~108~~, plotted over that same 5500 degrees of phase shift with respect to the reference clock. The lower plot demonstrated the synthesis of a lower frequency from the high speed reference clock.

The paragraph bridging pages 11 and 12, page 11, paragraph 2, lines 20 to 23 and page 12, paragraph 1, lines 1 to 12, insert the following paragraph.

The frequency step size of this invention depends on the frequency and the number of bits n in the accumulator math. It is coarser at frequencies closer to the reference clock frequency, and finer at lower frequency outputs. The worst case step size is the reference frequency divided by 2^n ~~2^n~~, where n is equal to the number of bits in the accumulator math. In the example of Table 1, the step size is 1000 MHz divided by 2^n. This gives a step size of approximately 244 kHz ~~KHz~~. To improve the frequency resolution an increased number of bits

in the math can be used. For example with 16 bit math, the frequency resolution improves to approximately 15.2 kHz ~~KHz~~. Increasing n to 32 bits would result in approximately 0.2Hz frequency resolution. It is only necessary to increase the number of bits of resolution in the adder/accumulators ~~102~~ 102a, 102b, and not necessarily the LUTs ~~105~~ 105a, 105b and the programmable dividers ~~106~~ 106a, 106b. The remaining least significant bits can be truncated before the LUTs ~~105~~ 105a, 105b with negligible effect on the RF output ~~108~~ phase noise quality. This means that very fine frequency resolution is achieved with negligible degradation in the phase noise. It can also be seen that the increment values 101 can be changed to provide an essentially instantaneous frequency change.

The paragraph bridging pages 12, 13 and 14, page 12, paragraph 2, lines 13 to 23 and page 13, paragraph 1, lines 1 to 23 and page 14, paragraph 1, lines 1 to 2 insert the following paragraph.

Phase modulation is added by the addition of a second adder 120. This adder is also high speed and runs at full rate. This modulation adder 120 adds the desired phase offset to the value of the accumulator ~~value~~ ~~102~~ 102a, 102b to provide a new increment value that is sent to the look up tables ~~105~~ 105a, 105b and the pulse swallow circuit ~~104~~ 104a, 104b. The number added could be positive or negative. The average value added is always zero over a long period of time. This ensures the overall effect of the modulation adder is only a phase modulation and not a change in the center frequency of operation. Compared to the reference clock frequency, the modulation information (122,123) is at a much lower frequency baseband rate. Figure 4 illustrates an

example of the incoming sampled baseband using 8 samples per symbol. Graph 200 is the desired phase rate signal control. Graph 201 is the sampled input. If the graph 201 is placed through a reconstruction filter the desired shape 200 will be produced. This is illustrated in spectrum plot of figure 6. The energy of the sampled waveform 201 is spread over the desired baseband 400 and the clock 404 and aliasing components 402 and 403. A low pass filter 401 is used in prior art, after a DAC to remove the undesired clock 404 and aliasing components 402 and 403. However, in the present invention there is no DAC as the phase modulation is achieved by directly adding digitally to the increment value. There is no place to put an analog low pass filter. This would result in clock and aliasing signal components showing up in the RF output 150. To overcome this problem an interpolator 121 is used to reduce the clock and aliasing signals as well as to shift their frequency so that they may be filtered at the RF output 150 using an optional band bass filter 109. The preferred embodiment of the interpolator is a linear interpolator. However, it is also valid to use other interpolation techniques such as (sin x)/x ~~sin x/x~~ interpolation and filtering. Sin x/x interpolation is well understood by those knowledgeable in the art. Linear interpolation is implemented by drawing a straight line between two known points. This is simple to implement as the increment value required for each reference clock cycle is based on the equation: Input sample frequency 122 divided by the clock reference frequency 103 multiplied by the difference of two adjacent sampled data point values. An implementation of the interpolator 121 used for suppressing the clock and aliasing components is shown in Figure 5.

The linear interpolated curve 301 now has more power in the desired curve 300 than the non interpolated curve 201. A full (sin x)/x ~~sin x/x~~ interpolater would remove the clock and aliasing component as the phase adjust would occur at every reference clock edge. This alleviates the need for any reconstruction filter which is now replaced with a full digital solution that can be implemented using an ASIC.

Page 14, paragraph 2, lines 3 to 16 insert the following paragraph:

Another advantage of the present device is that the output signal frequency 150 range is very wide. The pulse swallow ~~104~~ 104a, 104b circuit can block multiple reference clock pulses extending the programmable delay indefinitely. This is only limited by the number of overflow bits and math bits used. The output frequency range coverage can thus be from DC up to the high speed reference clock frequency. It is desirable to have as high a reference clock frequency as possible. A higher reference clock frequency extends the useful frequency range, and improves the frequency resolution. The upper reference frequency limit of the design is mostly limited by the design speeds of the high speed adders/accumulator ~~102~~ 102a, 102b and look up tables ~~105~~ 105a, 105b. It is understood in the art that speeds can be increased by parallel processing and other design techniques. For example multiple high speed adders/accumulator, LUTs or programmable delay lines could be used in parallel for increasing the speed and hence the output signal frequency capability of the invention.

Page 15, paragraph 2, lines 10 to 13 insert the following paragraph:

Within the spirit of the invention it is also possible to remove the adder/accumulators ~~(102)~~ 102a, 102b) and replace the LUT ~~(105)~~ 105a, 105b with a larger LUT. A simple counter could increment the values in the LUT. The LUT ~~(105)~~ 105a, 105b would in this case hold the pre-added values, and just cycle through them until the pattern repeats.

The paragraph bridging pages 15 and 16, page 15 , paragraph 5, lines 22 to 23 and page 16, paragraph 1, lines 1 to 3, insert the following paragraph.

It is possible to use a selection of different lookup tables ~~(105)~~ 105a, 105b or offset values to compensate for the temperature effect on the programmable delay lines ~~(106)~~ 106a, 106b. It is also possible to vary the implementation of the delay lines by altering the input clock signal. Examples of clock alteration would include frequency multiplication, division, or phase shifting.